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It focuses solely on deep-submicron CMOS devices, the workhorses of today's digital integrated circuits. A simple transistor model for manual analysis, called the unified MOS model, has been developed and is used throughout. Design Examples stress the design of Digital ICs from a real-world perspective.

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Digital Integrated Circuits: A Design Perspective J. Rabaey, A. Chandrakasan, and B. Nikolic 2nd edition Web Page. References: CMOS Digital Integrated Circuits: Analysis and Design S-M. Kang and Y. Leblebici 3rd edition . CMOS VLSI Design - A Circuits and Systems Perspective N. H. Weste and D. Harris 3rd edition . Midterm: Mon 5/2/11 in class.

EEEC118 - Digital Integrated Circuits

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1 EE134 1 Digital Integrated Circuit (IC) Layout and Design - Week 10, Lecture 20 Midterm Due in Class Dynamic Logic SRAM Wrap up EE134 2 Clocked CMOS Logic (C2MOS) Clocked CMOS Register (Positive Edge) ϕ 1 high: • Master Hi-Z state (N1 floating D n). • Slave enabled. Q n+1 = D n. ϕ 1 low: • Master enabled. N1 = D. M1 & M3 on.

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Rabaey, Chandrakasan & Nikolic, Digital Integrated ...

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